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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,887	08/25/2003	Tange Nan Barbour	BUR920030044US1	1886

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EXAMINER	
TU, CHRISTINE TRINH LE	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,887	BARBOUR ET AL.	
	Examiner	Art Unit	
	Christine T. Tu	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/7/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1-21 are objected to because of the following informalities:

Claim 1:

At line 1, the phrase "What is claimed is: " should be deleted.

At line 14, the use of parenthesis "(...)" should be avoided because it is not clear whether any limitation inside the parenthesis is actually being claimed.

At line 14, the use of capitalization of a term "DEFECTS" should also be avoided because it is not clear whether a capitalized word signifies a meaning other than the general meaning without the capitalization.

At lines 10-14, it is still not clear how a minimum amount of the post production test required can be determined in order to achieve optimum reliability of the integrated circuit (IC) based on the number of defective cells or active elements containing defective cells.

Claim 7:

At lines 10-14, it is still not clear how a control means can determine a minimum amount of the post production test required in order to achieve optimum reliability of the IC even based on the number of defective cells or active elements containing defective cells.

Claim 11:

At line 2, the word "stress" should be deleted.

Claim 13:

At lines 7-11, it is still not clear how a control means can determine a minimum amount of the post production test required in order to achieve optimum reliability of the IC even based upon the accumulated count.

Claim 16:

At lines 7-9 and 10, the use of capitalization of a term "DEFECTS" should also be avoided because it is not clear whether a capitalized word signifies a meaning other than the general meaning without the capitalization.

At lines 11-14, it is still not clear how a minimum amount of the post production test required can be determined in order to achieve optimum reliability of the IC based on the number of defective cells or active elements containing defective cells.

Claim 19:

At lines 10-14, it is still not clear in what explicitly way is to be consider as accurately determining a minimum amount of the post production test required in order to achieve optimum reliability of the IC using the location.

Claims 2-6, 8-10, 12, 14-15, 17-18 and 20-21:

These claims are objected because they depend on claims 1, 7, 13, 16 and 19 and contain the same problems of indefiniteness.

Appropriate correction is required.

2. The following rejections are based on the best understanding of the claimed invention by the examiner in view of the ambiguities that exist in the claims as mentioned above (supra ¶1).

3.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hill et al. (6,141,779 and Hill hereinafter).

Claim 1:

Hill teaches the invention substantially as claimed. Hill teaches (figures 1 & 3) that an IC (125) includes a built-in self-test (BIST) engine (130) for testing memory array (102) for faults. The BIST engine (130) is hardware for controlling the execution of on-chip memory tests that are designed to detect and locate failures in cells (104) of memory array 9102). The BIST engine (130) generates test patterns and corresponding expected output data for memory 9100). A comparator (132) compares the output data DATA_OUT [0:N-1] with the expected data value present in expected data register (140). If comparator (132) detects a bit mismatch, the corresponding bit in sticky compare register (142) which also corresponds to the column in memory array (102) that generated the mismatch, is set to a "1". Upon completion of the BIST test, each "1" in sticky compare register (142) corresponds to a column in the memory array (102) that contains a failed cell (104). Later, the contents of sticky compare register (142) are right shifted and a counter (144) is incremented once per shift cycle until the right most bit of the sticky compare register (142) contains a 1 or until N shift cycles have completed, whichever occurs first (figures 1 & 3, column 5 lines 38-column 6 line 27).

Hill does not explicitly teach the determination of a minimum amount of post production testing required on the IC device to achieve optimum reliability of the IC

device. Hill, however, teaches that the counter (144) contains the encoded RAM redundancy map value MAP and loaded into a non-volatile storage (146) (column 6 lines 3-10).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Hill's IC also including the feature of determining a minimum amount of post production testing required on the IC to achieve the reliability of the IC. One having ordinary skill in the art would be motivated to realize so because the RAM redundancy map is later d3ecoded and constructed from the contents of the register (146) for correcting memory array (102) (column 6 lines 16-27).

Claim 2:

Hill does not explicitly teach the testing is stress testing. It would have been obvious to one skilled in the art to realize that Hill's BIST engine (130) would have been comprised the features of stress testing for testing the memory array (102). One having ordinary skill in the art would be motivated to realize so because testing a memory array in an IC by using stress test is well-known in the art.

Claim 3:

Hill teaches that N columns (COL[0], ..., COL[n-1]) of the array (102) can be activated (figure 1, column 4 lines 9-13).

Claim 4:

Hill teaches a redundant column (COL[N]) is implement adjacent to the N-1th column of memory array (102) (figure 1, column 4 lines 13-17; column 6 lines 39-42).

Claims 5-6:

Due to the similarity of claims 5-6 to claims 2-3, these claims are also rejected under the same rationale applied against claims 2-3.

Claims 7-12:

Claims 7, (8-9 & 11-12) and 10 are rejected for reasons similar to those set forth against claims 1, (2-3) and 4, respectively.

Claim 13:

Hill teaches that the sticky compare register (142), which corresponds to the column in the memory array (102), is set to "1" when a mismatch occurs. Then the contents of the sticky compare register 9142) are right-shifted and a counter (144) is incremented once per shift cycle, until N shift cycles have completed (column 5 lines 54-column 6 line 7).

Claims 14-15:

Due to the similarity of claims 14-15 to claims 2-3, these claims are also rejected under the same rationale applied against claims 2-3.

Claim 16:

This claim is similar to claim 1 except that the features are in instructions which being stored in computer program product. Hill, however, teaches that the BIST engine (13) can be firmware (column 5 lines 40-41).

Claims 17-18 and 20-21:

Due to the similarity of claims (17-18 & 20-21) to claims 2-3, these claims are also rejected under the same rationale applied against claims 2-3.

Claim 19:

Hill's sticky compare register (142) will contain a "1" in the bit corresponding to column COL[1] if COL[1] is determined to be the only defective column (column 6 lines 27-32).

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christine T. Tu
Primary Examiner
Art Unit 2133

September 16, 2005